REMARKS

Claims 3, 5-11, 14, 16-22, 25, and 27-33 are pending in the application. The Examiner's reconsideration of the rejections in view of the amendments and remarks is respectfully requested.

Claims 31 and 32 have been rejected under 35 USC 101, as being directed to non-statutory subject matter. The Examiner stated essentially that there is no clear result - that the application of storage of the address is not clear.

Claims 31 and 32 have been amended to include, essentially, "accessing the vector data file for" a data vector or storage element, respectively. Accordingly, Claims 31 and 32 are believed to include a result, an access of the vector data file. Reconsideration of the rejection is respectfully requested.

Claims 3, 8, 9-11, 14, 19-22, 25 and 31-33 have been rejected under 35 USC 103(a) as being unpatentable over Fossum et al. (USPN 4,888,679) in view of Birrittella (USPN 6,266,759). The Examiner stated essentially that the combined teachings of Fossum and Birrittella teach or suggest all of the limitations of Claims 3, 8, 9-11, 14, 19-22, 25 and 31-33.

Claims 3, 9, 10, 11, 14 25, and 31-33 are the independent claims.

Claims 3, 9, 10, and 11 recite, *inter alia*, "a pointer array electrically coupled by a bus to the vector data file, the pointer array including a plurality of entries wherein each entry identifies at least one storage element in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, wherein

the words are addressed by a word address decoder coupled to the pointer array." Claims 14, 25 and 31-33 claim, *inter alia*, "providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for at least one particular entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file."

Fossum teaches a vector stored in main memory (see FIG. 3) addressed by an address register and adder (see col. 8, line 60 to col. 9, line 15). Fossum does not teach or suggest that "entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file" as claimed in Claims 3, 9, 10, 11, 14 25, and 31-33. Consider first that the vector of Fossum is not a vector data file - the vector of Fossum is merely vector in main memory. Further, entries in a address register of Fossum are not grouped into addressable words. The address register of Fossum is used in calculating addresses of vector elements using an adder or length counter. The calculating of individual vector elements is not analogous to an addressable word. Therefore, Fossum fails to teach all the limitations of Claims 3, 9, 10, 11, 14 25, and 31-33.

Birrittella teaches multiple overlapped vector memory-reference instructions (see Abstract). Birrittella does not teach or suggest that "entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file" as claimed in Claims 3, 9, 10, 11, 14 25, and 31-33. Birrittella teaches that a vector unit calculates memory addresses for

vector memory-reference instructions (see col. 3, lines 42-45). Similar to Fossum, Birrittella's calculation is not analogous to an addressable word corresponding to a vector, essentially as claimed in Claims 3, 9, 10, 11, 14 25, and 31-33. Therefore, Birrittella fails to cure the deficiencies of Fossum.

The combined teachings of Fossum and Birrittella teach a method for calculating addresses of vector memory-reference instructions. The combined teachings of Fossum and Birrittella fails to teach or suggest "entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file" as claimed in Claims 3, 9, 10, 11, 14 25, and 31-33.

Claims 7, 16-18, 29 and 30 have been rejected under 35 USC 103(a) as being unpatentable over Fossum in view of Birrittella as applied to Claims 3, 14 and 25, and further in view of Sakakibara (USPN 5,392,443). The Examiner stated essentially that the combined teachings of Fossum, Birrittella and Sakakibara teach or suggest all of the limitations of Claims 7, 16-18, 29 and 30.

Claim 7 depends from Claim 3. Claims 16-18 depend from Claim 14. Claims 29 and 30 depend from Claim 25. The dependent claims are believed to be allowable for at least the reasons given for the respective independent claims. Reconsideration of the rejection is respectfully requested.

Claims 5, 6, 27 and 28 have been rejected under 35 USC 103(a) as being unpatentable over Fossum in view of Birrittella as applied to Claims 3, 14 and 25, and further in view of Sakakibara (USPN 5,392,443). The Examiner stated essentially that the combined teachings of

Fossum, Birrittella and Sakakibara teach or suggest all of the limitations of Claims 5, 6, 27 and 28.

Claims 5 and 27 are the independent claims.

Claim 5 claims, *inter alia*, "a pointer array electrically coupled by a bus to the vector data file, the pointer array including a plurality of entries wherein each entry identifies at least one storage element in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, wherein the words are addressed by a word address decoder coupled to the pointer array." Claim 27 claims, *inter alia*, "providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for at least one particular entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file."

As presented above, the combined teachings of Fossum and Birrittella fails to teach or suggest that "entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file."

Sakakibara fails to cure the deficiencies in the combined teachings of Fossum and Birrittella in this regard; Sakakibara teaches that a vector register unit 170 holding actual vector elements (see col. 11, lines 33-40). The vector register unit does not store entries or pointers to a vector data file, essentially as claimed. Indeed, nowhere does Sakakibara teach or suggest the use of a pointer array, much less entries identifying at least one storage element in the vector data file. Therefore, Sakakibara fails to cure the deficiencies in the combined teachings of Fossum

and Birrittella.

The combined teachings of Fossum, Birrittella and Sakakibara fail to teach or suggest that "entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file" as claimed in Claims 5 and 27.

Claims 6 and 28 depend from Claims 5 and 27, respectively. The dependent claims are believed to be allowable for at least the reasons given for the respective independent claims. Reconsideration of the rejection is respectfully requested.

For the forgoing reasons, the application, including Claims 3, 5-11, 14, 16-22 and 25, 27-33, is believed to be in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,

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